CEL 2 & ETL 2: Analog and Digital Systems

T005

Friday, 01/11/2013
8:30 - 11:30 AM

WORKFORCE DEVELOPMENT AUTHORITY

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ADVANCED LEVEL NATIONAL EXAMINATIONS, 2013, TECHNICAL AND PROFESSIONAL TRADES

EXAM TITLE : Analog and Digital Systems

OPTIONS: - **Computer Electronics (CEL)**

- **Electronics and Telecommunication (ETL)**

DURATION: **3hours**

INSTRUCTIONS:

The paper contains **three (3)** sections :

Section I: Fourteen **(14)** questions, all **Compulsory**; **55marks**

Section II: Five **(5)** questions, **Choose any three (3)**; **45marks**

Section III: Three **(3)** questions, **choose any ONE (1)** **15marks**

Section I: All the 14 questions are compulsory 55marks

01. Define the following terms : **3marks**

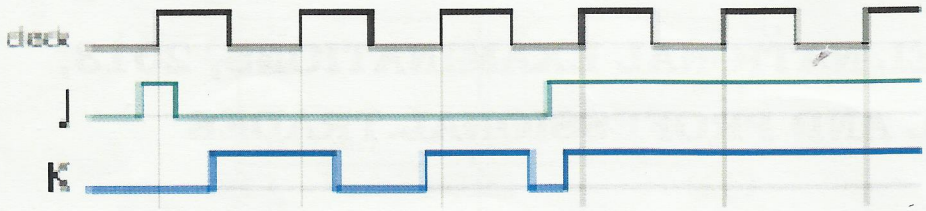
a. Code converter
b. A flip-flop
c. Modulus of a counter

02. Minimize the following Boolean expressions by using karnaugh map (k.map).

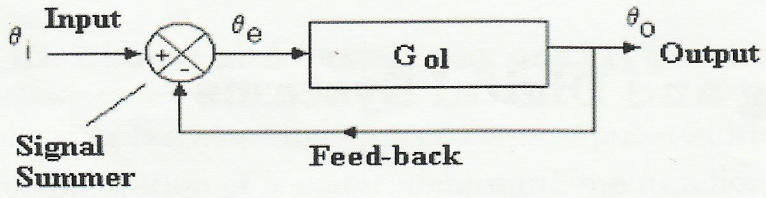
$F(W,X,Y,Z) = \Sigma m(0,1,2,4,5,6,8,9,12,13,14)$

$F = \overline{A}\,\overline{B}\,\overline{C} + \overline{B}C\overline{D} + A\overline{B}\,\overline{C} + \overline{A}BC\overline{D}$ **2marks**

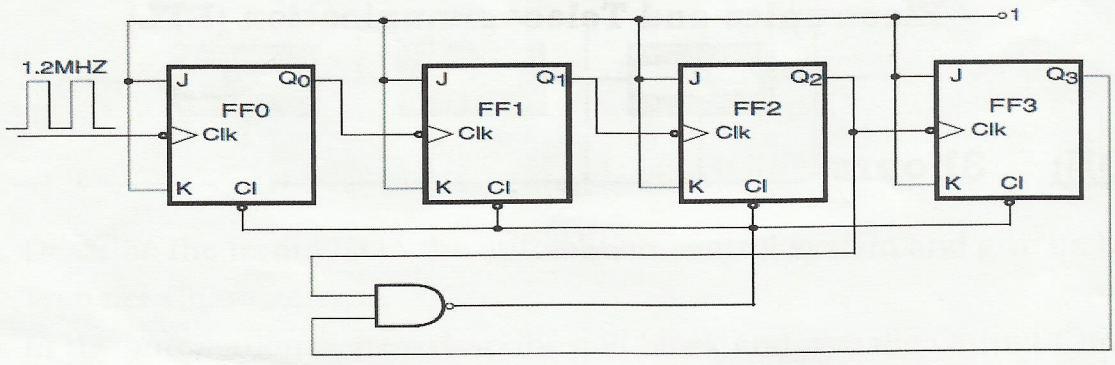
03. Learn the JK flip-flop waveform below and draw out the corresponding waveform of Q and $\overline{Q}$. Assume that at the initial the Q =0 (Low state). The clock signal is activated on High-to-Low transition. **2marks**



04. Find out the transfer function of the closed loop control system below. **3marks**



05. Refer to the binary ripple counter of figure shown below; determine the modulus of the counter and also the frequency of the flip-flop Q3 output. **6marks**



06. What are the methods for obtaining sine wave output from an inverter? **5marks**

07. What are the main blocks of a switched mode power supply (SMPS)? **5marks**

08. Identify different types of inverters or DA-AC converters. **6marks**

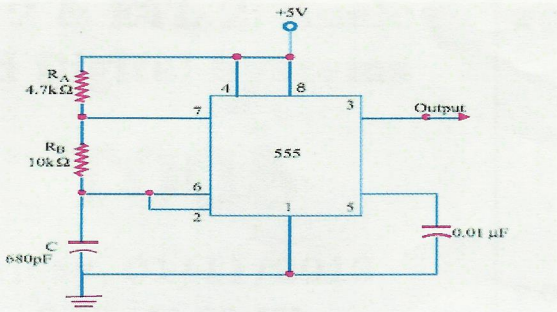
09. Identify two (2) among different types of protection functions that a series-pass transistor voltage regulator can include. **2marks**

10. Identify different types of memories based on the way data access the memory. **4marks**

11. Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: V_{IL}=1.5V; V_{OL}=0.5V; V_{IH}=3.5V and V_{OH}=4.4V. Determine the noise margins. **6marks**

12. What are the two main difficulties of variable frequency system? **2marks**

13. Refer to this figure below,



Calculate: a) The Discharging time (T_{OFF}) b) The charging time(T_{ON})
c) The oscillation time(Period), d) The oscillation frequency
e) The duty cycle **5marks**

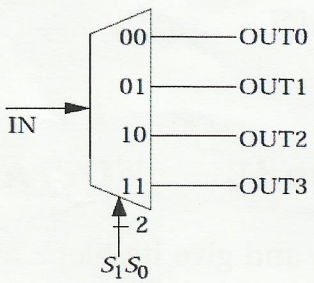
14. The speed of an electric motor is directly proportional to voltage such that N=20V where V is Volts and N in rev/min. The motor is controlled by a power supply which has an output voltage related to the position of the control knob by V=2φ (in degrees). Draw the block diagram and deduce the overall transfer function. Determine the output speed when the knob is set to 60°. **4marks**

Section II. Choose and answer any three (3) questions. 30marks

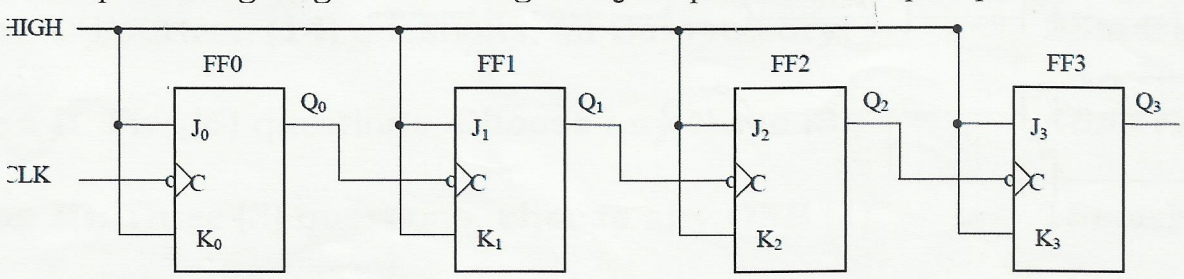
15. Clearly describe the working principle of 555 timers by using internal equivalent circuit **10marks**

16. a) Identify the main components of a programmable Logic Controller (PLC). **9marks**
b) What is a Ladder Logic? **1mark**

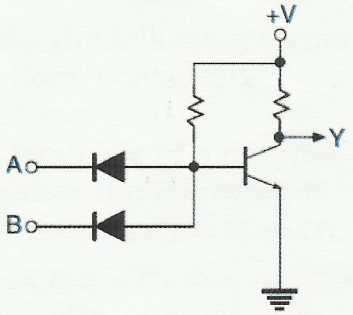
17. Identify the function represented by the module shown below. Determine the Boolean expression of each output and implement it using only NAND gates. **10marks**



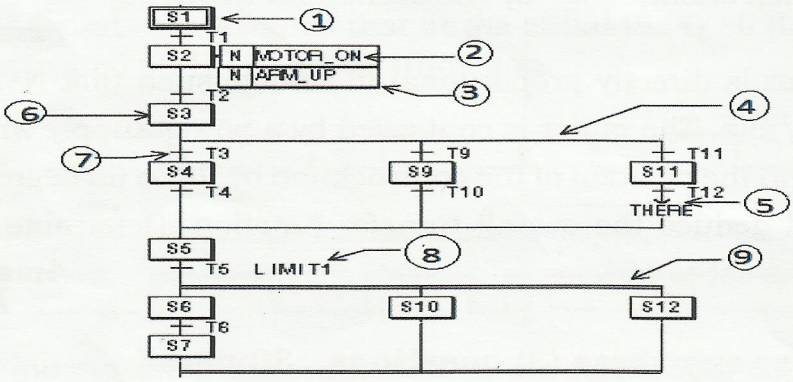
18. Consider the circuit shown below and answer to following questions : **10marks**
a) What type of circuit is represented?
b) If each flip-flop has a propagation delay of 10ns, determine the total propagation delay time.
c) Determine the maximum frequency (in MHz) at which the circuit is operated.
d) Develop a timing diagram showing the Q output of each flip-flop.



19. a. Give the function performed by the following circuit. **1mark**

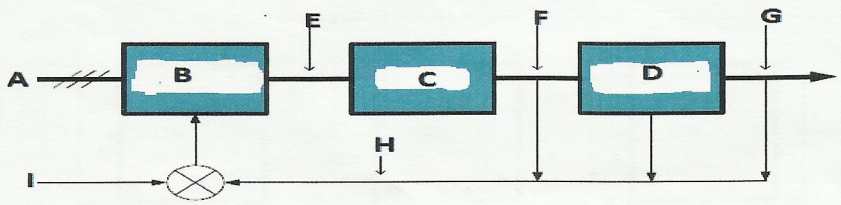


b. Describe each part of the following SFC. **9marks**



Section III. Choose and answer any one (1) question 15marks

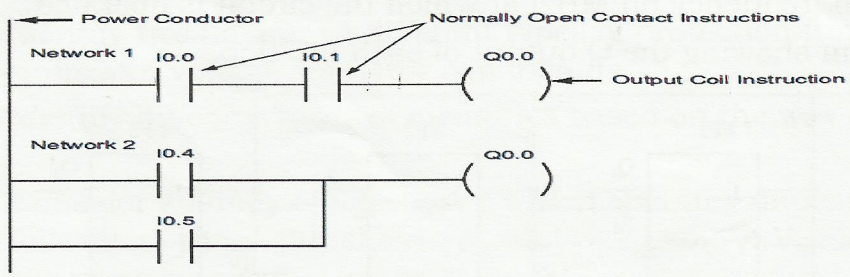
20. The following is a block diagram of a typical pulse width modulation adjustable speed drive configuration of a motor; determine the function or variable type represented on the diagram by letters A, B, ..., I and specify the six (6) basic protections that must be performed on such circuit. **15marks**



21: a. Describe the term PID in the automation control system and give its block and Transfer Characteristic. **8marks**

b. In the automation system describe a PI block and give the Output Characteristics of it. **7marks**

22. After analyzing and giving the function of the following ladder diagram, convert it into **STL and FBD.** **15marks**



SECTION I.

Q1. a) Code Converter: is a combinational logic circuit that changes data presented in one type of binary code to another type of binary code. 1

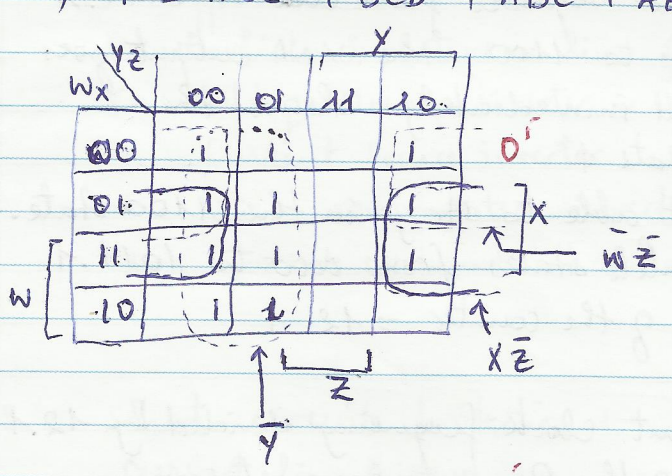
b) Flip-Flop: is a binary storage device that is capable of storing one bit of information. 1
or It is a sequential circuit that has two stable states (high and low).

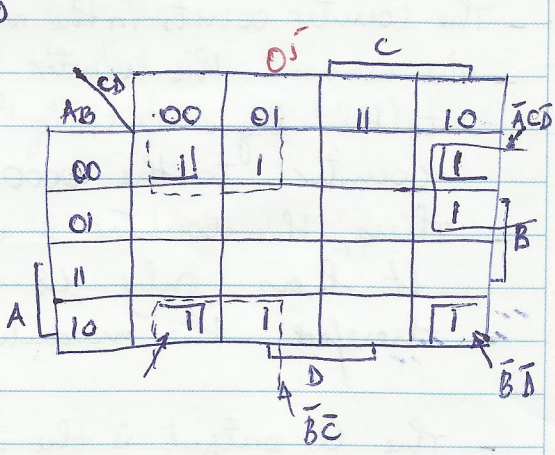
3marks.

c) The modulus (mod number) of a counter: is the number of different logic states it goes through before it comes back to the initial state to repeat the count sequence. 1

Q2. a) $F(w, x, y, z) = \Sigma_m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$.

b) $F = \bar{A}\bar{B}\bar{C} + \bar{B}C\bar{D} + A\bar{B}\bar{C} + \bar{A}BC\bar{D}$



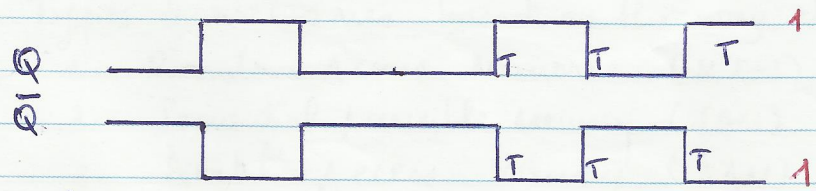


2marks.

$F = \bar{y} + \bar{w}\bar{z} + x\bar{z}$ 0'

$F = \bar{B}\bar{D} + \bar{B}\bar{C} + \bar{A}C\bar{D}$ 0'

Q3. When the clock is activated on low to high:

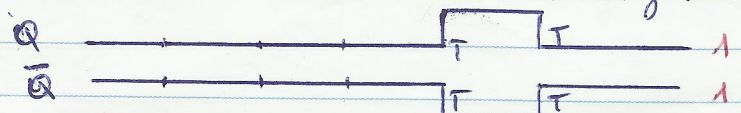


1 1

T: Toggle.

2marks.

OR. When the clock is activated on High to low.



1 1

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04. $G_{ol} = \frac{\theta_o}{\theta_e}$ 0½

$\theta_e = \theta_i - \theta_o$ 0½

$G_{ol} = \frac{\theta_o}{\theta_i - \theta_o}$

$G_{ol}(\theta_i - \theta_o) = \theta_o$

$G_{ol}\theta_i - G_{ol}\theta_o = \theta_o$

$G_{ol}\theta_i = \theta_o + G_{ol}\theta_o$

$G_{ol}\theta_i = \theta_o(1 + G_{ol})$ 0½

$G_{cl} = \frac{\theta_o}{\theta_i}^{0½} = \frac{G_{ol}}{1+G_{ol}} = \frac{1}{\frac{1}{G_{ol}}+1}$ 1

G_{ol}: G open loop
G_{cl}: G closed loop.

3marks

05. - The counter counts in the natural sequence from 0000 to 1111. 1
- the moment the counter goes to 1100, the NAND output goes to the logic '0' state and immediately clears the counter to the 0000 state. 1
- Thus, the counter is not able to stay in the 1100 state. It has only 12 stable states from 0000 to 1011. 1
- Therefore, the modulus of the counter = 12. 1

6marks

- The Q_3 output is the input clock frequency divided by 12. 1
- Therefore, the frequency of the Q_3 output waveform

$= \frac{1.2 \times 10^3}{12} = 10^5 Hz = 100 KHz$. 1

06. Methods for obtaining sine wave output from inverter:

1. Resonating the load 1
2. Using proper filters 1
3. Using pulse width modulation 1
4. Using sine wave synthesis 1
5. Using polyphase inverters. 1

5 marks.

07. Main blocks of a SMPS.

1. Input rectifier and filter 1
2. High frequency switch 1
3. Power transformer 1
4. Output rectifier and filter 1
5. Control circuit. 1

5marks.

08. Classification of inverters (DC - AC converters).

1. Single phase inverter 1
2. Three phases inverter 1
3. offline inverters or autonomous inverters 1
4. Online inverters or line-fed inverters 1
5. Voltage source inverter or voltage stiff inverter (VSI) 1
6. Current source inverter 1
7. Line commutated inverter 1
8. Forced commutated inverter 1

6marks

Consider only six.

09. - Short-circuit protection 1
- Current limiting 1
- Thermal shut down 1
- Over-voltage protection 1

Consider only two

2marks.

10. Types of memories based on the way data access them.

1. Random Access Memories (RAM) 1
2. Sequential Accessible Memory (SAM) 1
3. Direct Access Memory (DAM) 1
4. Content Addressable Memory (CAM) 1

4marks.

11. The noise margins are given by:

$NM_0 = V_{IL} - V_{OL}$ 1

$= 1.5 - 0.5$ 1

$= 1\,V$ 1

$NM_1 = V_{OH} - V_{IH}$ 1

$= 4.4 - 3.5$ 1

$= 0.9\,V$ 1

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6 marks.

12. Two main difficulties of variable frequency system:

1- Control of V requires variation of chopper frequency over a wide range. 1

2- Filter design for variable frequency operation is difficult. 1

2 marks

13. $T_{OFF}: t_1 = 0.7\,R_B C$ OJ

$= 0.7 \times (10\times10^3) \times (680\times10^{-12}) = 4.76\times10^{-6}\,s = 4.76\,\mu s$ OJ

$T_{ON}: t_2 = 0.7\,(R_A + R_B)\,C$ OJ

$= 0.7\,((4.7\times10^3) + (10\times10^3)) \times (680\times10^{-12}) = 6.99\times10^{-6}\,s = 6.99\,\mu s$ OJ

5 marks.

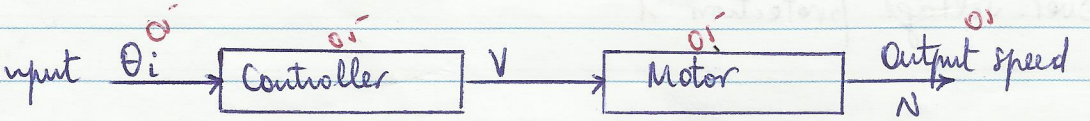
Period: $T = t_1 + t_2$ OJ $= 4.76 + 6.99 = 11.757\,\mu s$ OJ

$f = \frac{1}{T}$ OJ $= \frac{1}{11.757\times10^{-6}} = 8.5\times10^4 = 85$ OJ KHz.

Duty cycle: $\frac{t_{ON}}{T} \times 100\% = \frac{6.997}{11.757} \times 100\% = 59.5\%$ OJ.

Note: $\ln 2 = 0.69 \simeq 0.7$

14.



OJ OJ OJ OJ

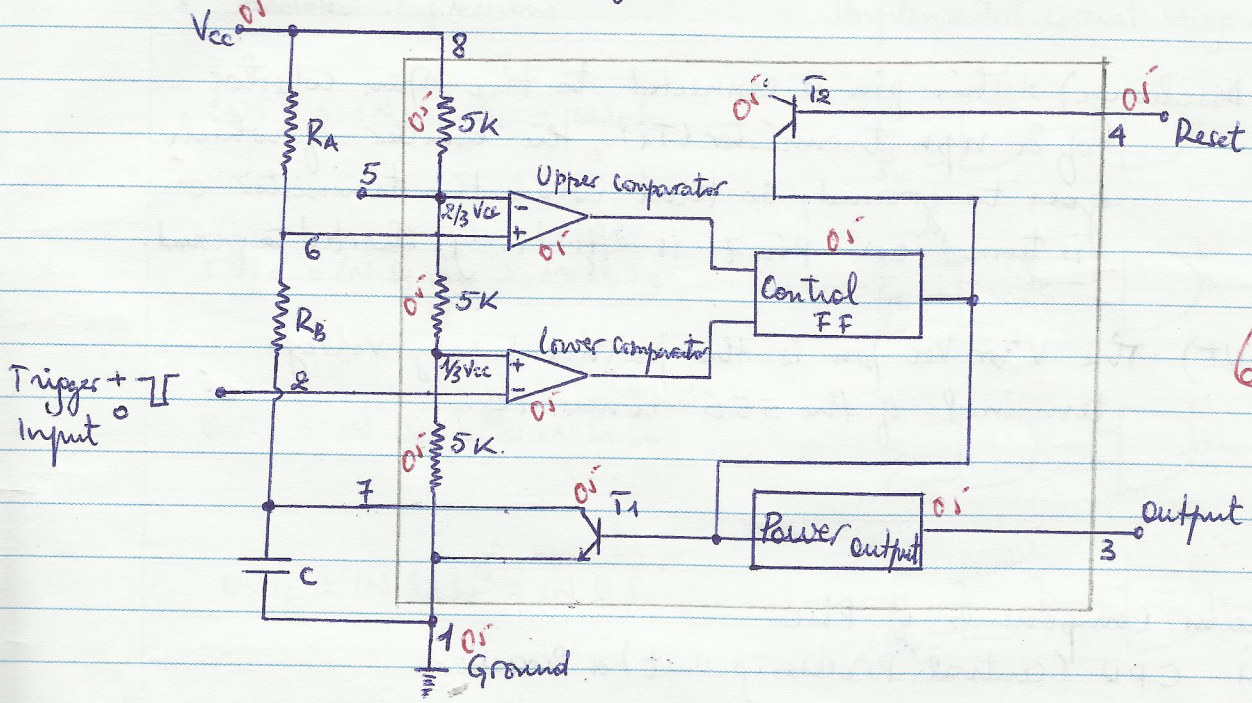
4 marks.

Transfer function: $G = \frac{N}{\theta_i}$ OJ $= 2\theta_i \times 20 = 40$ OJ rev/min per degree

Output speed: $N = 40 \times 60 = 2400$ 1 rev/min.

SECTION II.

15. Internal Schematics of 555 timer.



6 marks

Pin Functions:

Pin 1 (Ground): The ground (or common) pin is the most-negative supply potential of the device, which is normally connected to circuit common (ground) when operated from positive supply voltages.

Pin 2 (Trigger): This pin is the input to the lower comparator and is used to set the latch, which in turn causes the output to go high.

Pin 3 (output): The output of the 555 comes from a high-current totem-pole stage made up of transistors T_1 - T_2.

Pin 4 (Reset): This pin is also used to reset the latch and return the output to a low state.

Pin 5 (control voltage): This pin allows direct access to the $\frac{2}{3}V^+$ voltage-divider point, the reference level for the upper comparator.

Pin 6 (Threshold): Pin 6 is one input to the upper comparator (the other being pin 5) and is used to reset the latch, which causes the output to go low. 0½

Pin 7 (Discharge): This pin is connected to the open collector of a npn transistor (T_1), the emitter of which goes to ground, so that when the transistor is turned 'ON' Pin 7 is effectively shorted to ground. 0½

Pin 8 (V^+): The V^+ or Vcc pin is the positive supply voltage terminal of the 555 timer IC. 0½

16. a) Main Components of PLC

1. CPU (Central Processing Unit) or Processor 1
2. Memory (RAM and ROM) 1
3. Input module 1
4. Output module 1
5. Communication Interface 1
6. Analog / Digital converter 1
7. Display monitor 1
8. Address bus 1
9. Data bus 1
10. Power supply

10 marks.

b) Ladder logic: is the main programming method for PLC. 1

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17. * The function represented is a demultiplexer with IN as input, $S_1 S_0$ as data selector and OUT_0, OUT_1, OUT_2, OUT_3 as outputs. 2marks this.

* Boolean expressions

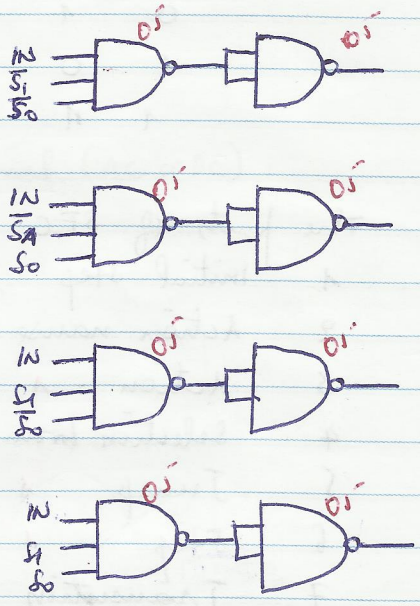
$OUT0 = IN \cdot \bar{S}_1 \cdot \bar{S}_0 = \overline{\overline{IN \bar{S}_1 \bar{S}_0}}$

$OUT1 = IN \cdot S_1 \cdot \bar{S}_0 = \overline{\overline{IN S_1 S_0}}$

$OUT_2 = IN \cdot S_1 \cdot \bar{S}_0 = \overline{\overline{IN S_1 \bar{S}_0}}$

$OUT_3 = IN\, S_1 S_0 = \overline{\overline{IN S_1 S_0}}$

* Implemented circuit using NAND.



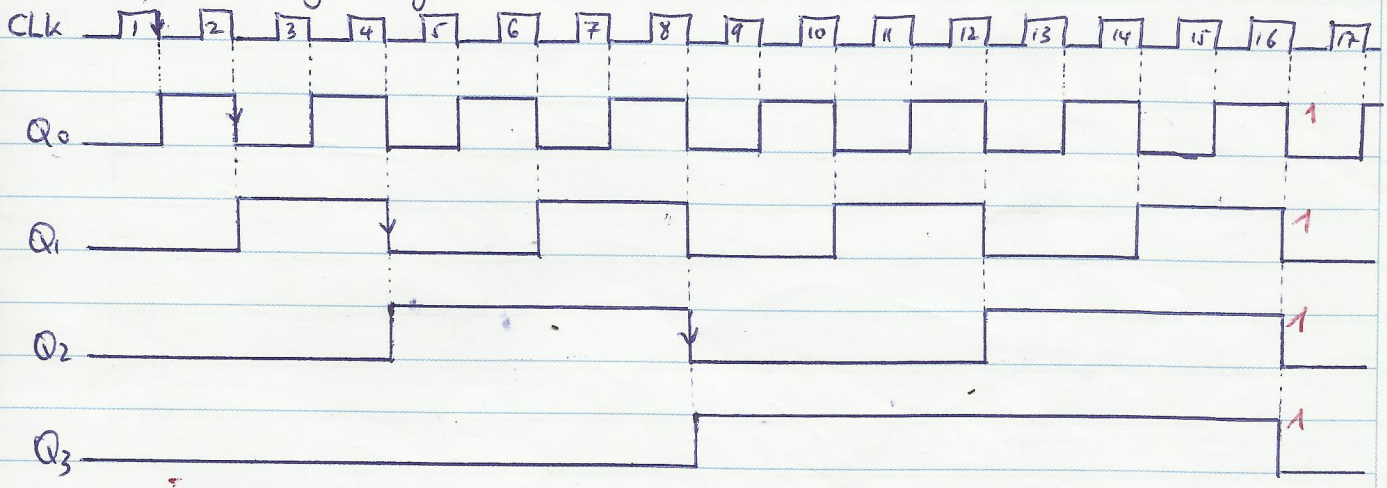
10marks

18. a) The circuit represented is a 4-bits asynchronous binary counter 1

b) Total propagation delay : $t_p = 4 \times 10ns = 40ns$. 1 1

c) Maximum frequency : $f = \frac{1}{t_p} = \frac{1}{40ns} = 25 MHz$. 1 1

d) Timing diagram



10marks

19. a) The function performed is the NAND gate, according to truth table below: 1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

b) The parts of SFC given are:

1 Initial step 1
2 Action name 1
3 Action 1
4 Selection branch 1
5 Jump 1
6 Step 1
7 Transition 1
8 Transition name 1
9 Parallel branch 1

10 marks

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SECTION III.

20.

A : Utility power or Input signal 1
B : Adjustable speed drive 1
C : Motor 1
D : Process equipment 1
E : Variable power or variable signal (AC or DC) 1
F : Variable speed 1
G : Process output / output signal 1
H : Appropriate feedbacks 1
I : Process reference. 1

15 marks

Protections :

1. Over current 1
2. Short circuit 1
3. Ground fault 1
4. over voltage 1
5. over temperature 1
6. Motor overload 1
7. Under voltage 1

consider six only:

~~21. a)~~

21.

a) PID Controller :

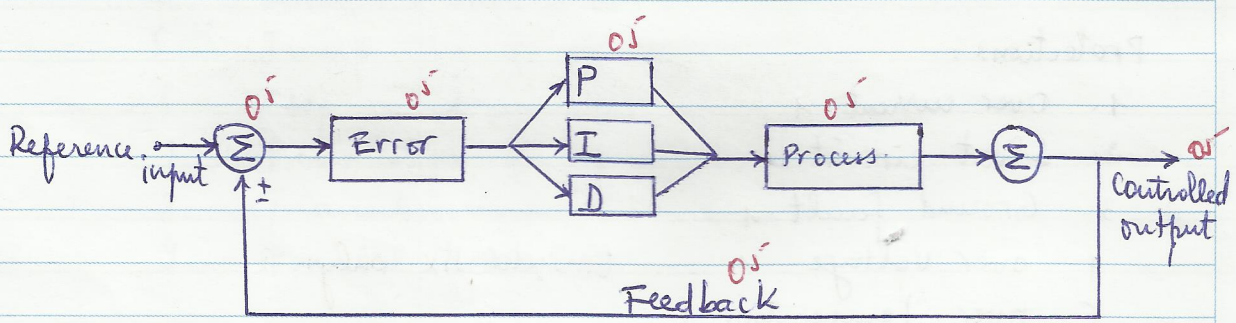
→ PID : Proportional Integral Derivative controller is a generic control loop feedback mechanism (controller) widely used in industrial control systems;

→ A PID is the most commonly used feedback controller;

→ A PID controller calculates an 'error' value as the difference between a measured process variable and a desired set point;

→ The controller attempts to minimize the error by adjusting the process control inputs.

A Block diagram of PID Controller :



Defining $u(t)$ as the controller output, the final form of PID algorithm is :

$$u(t) = MV(t) = K_p e(t) + K_i \int_0^t e(\tau)\,d\tau + K_d \frac{d}{dt} e(t).$$

Where

K_p : Proportional gain, a tuning parameter

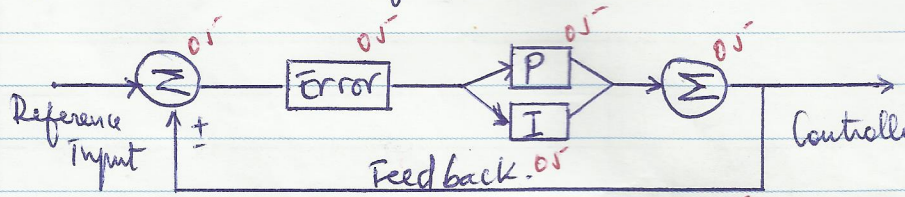
K_i : Integral gain, a tuning parameter

K_d : Derivative gain, a tuning parameter

$E \triangleq$ Error $= SP - PV$.

T : Time or Instantaneous time (the present).

b). Basic block of a PI controller :



A PI (proportional - Integral) Controller is a special case of PID Controller, in which the derivative (D) of the error is not used;

The controller output is given by $K_p \Delta + \int \Delta\,dt$

where Δ is the error or deviation of actual measured value (PV), from the setpoint (SP). $\Delta = SP - PV$.

22.

→ STL (Statement List) instructions include an operation and an operand.

→ The operation to be performed is shown on the left;

→ The operand, the item to be operated on, is shown on the right;

→ Feedback diagram (FBD) include rectangular functions, with inputs shown on the left side of the rectangular and outputs shown on the right side.

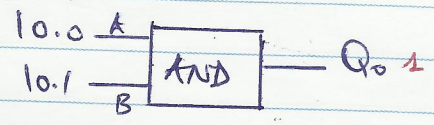
STL : Network 1

```
LD  I0.0
A   I0.1
=   Q0.0
```

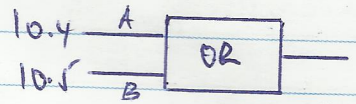
Network 2

```
LD  I0.4
O   I0.5
=   Q0.1
```

FBD : Network 1.



Network 2.



15 marks